The opinion in support of the decision being entered today is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte LUAN C. TRAN

Appeal 2007-2035
Application 09/848,846[1]
Technology Center 2800

Decided: October 2, 2007

Before KENNETH W. HAIRSTON, ROBERT E. NAPPI, and JOHN A. JEFFERY, *Administrative Patent Judges*.

JEFFERY, *Administrative Patent Judge.*

DECISION ON APPEAL

Appellant appeals under 35 U.S.C. § 134 from the Examiner's rejection of claims 11, 12, and 14. We have jurisdiction under 35 U.S.C. § 6(b). We reverse.

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[1] This application is a divisional of Application Serial No. 09/388,856, filed Sept. 1, 1999, now U.S. Pat. 6,579,751.

STATEMENT OF THE CASE

Appellant invented a method for forming integrated circuitry. In particular, memory and peripheral circuitry are formed over a semiconductor substrate. Using a common mask, a halo implant[2] is conducted so as to impart to at least three of the devices three different respective threshold voltages. To this end, the common masking step involves masking only portions of some of the devices which receive the halo implant.[3] Claim 11 is illustrative with the key limitation in dispute emphasized:

> 11. A semiconductor processing method comprising:
>
> a masking step providing a common mask; and
>
> an implant step carried out through the common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to *at least three of the devices three different respective threshold voltages*, wherein the common masking step comprises masking only portions of some of the devices which receive the halo implant, said portions comprising portions of peripheral circuitry devices.
>
> (Emphasis added.)

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[2] "Halo implants" are formed in MOSFETs by implanting dopants within a substrate proximate the source and drain regions, and are typically underneath the channel region. The implanted halo dopant raises the doping concentration only on the inside walls of the source/drain junctions, so that the channel length can be decreased without needing to use a higher doped substrate. As a result, deleterious effects of "punchthrough" (i.e., merging of the source and drain depletion regions) are minimized (Specification 2:2-18)

[3] *See generally* Specification P. 9, l. 1 - P. 10, l. 16.

The Examiner relies on the following prior art reference to show unpatentability:

Lowrey	US 5,252,504	Oct. 12, 1993

Claims 11, 12, and 14 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Lowrey.

Rather than repeat the arguments of Appellant or the Examiner, we refer to the Brief and the Answer for their respective details. In this decision, we have considered only those arguments actually made by Appellant. Arguments which Appellant could have made but did not make in the Brief have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

OPINION

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. *See In re Fine*, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the Examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17, 148 USPQ 459, 467 (1966).

Discussing the question of obviousness of a patent that claims a combination of known elements, *KSR Int'l v. Teleflex, Inc.*, 127 S. Ct. 1727, 82 USPQ2d 1385 (2007) explains:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, §103

> likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. *Sakraida* [*v. AG Pro, Inc.*, 425 U.S. 273, 189 USPQ 449 (1976)] and *Anderson's-Black Rock*[*, Inc. v. Pavement Salvage Co.*, 396 U.S. 57, 163 USPQ 673 (1969)] are illustrative—a court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.

KSR, 127 S. Ct. at 1740, 82 USPQ2d at 1396. If the claimed subject matter cannot be fairly characterized as involving the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement, a holding of obviousness can be based on a showing that "there was an apparent reason to combine the known elements in the fashion claimed." *Id.*, 127 S. Ct. at 1740-41, 82 USPQ2d at 1396. Such a showing requires "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. . . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *Id.*, 127 S. Ct. at 1741, 82 USPQ2d at 1396 (quoting *In re Kahn*, 441 F.3d 977, 987, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006)).

If the Examiner's burden is met, the burden then shifts to the Appellant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. *See In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

The Examiner's rejection indicates that Lowrey teaches a semiconductor processing method with every claimed feature including conducting a halo implant to devices formed over a substrate that is sufficient to impart two different threshold voltages to two different respective threshold voltages. According to the Examiner, Lowrey teaches every claimed feature except for three different devices having three different threshold voltages. The Examiner, however, concludes that such a feature merely duplicates parts and therefore is an obvious variation of Lowrey's teachings (Answer 3-4).

Appellant argues that the Examiner has simply not provided any reason or evidence as to why the skilled artisan would have included three different transistors with three different threshold voltages in Lowrey rather than two transistors (Br. 4-6).

The Examiner responds that it would have been obvious to form a third transistor with a third threshold voltage because DRAM devices may include hundreds of transistors, such as read-out transistors, which would have a third threshold voltage different from the peripheral and access transistors (Answer 6).

The sole issue before us, then, is whether it would have been obvious to the skilled artisan at the time of the invention to form a third device with a third threshold voltage in Lowrey via the claimed processing method. For the following reasons, we answer this question "no."

Lowrey discloses a CMOS integrated circuit (e.g., a DRAM) where a first layer of polysilicon 45 is deposited on a wafer 11 that forms transistor gates (Lowrey, col. 6, ll. 44-48; Fig. 6). The polysilicon 45 is patterned only in the n channel areas which are over p type material. A halo implant (or

"blanket implant") consisting of boron is applied. Because the polysilicon completely covers the n wells 21, the halo implant is effectively only applied to the p type material (Lowrey, col. 6, ll. 57-66; Fig. 6).

Although Lowrey does not actually show the halo implants in Figure 6, we presume that they would be implanted to the p type material in areas which are not directly underneath the polysilicon layer 45 (i.e., in the areas adjacent the n-wells 21). In this regard, we presume that the polysilicon layer 45 functions as the "common mask" as claimed.

It is undisputed that implanting this boron halo implant directly affects the device's threshold voltage. Furthermore, Lowrey discusses in the Background section that in DRAM applications, access devices generally need a higher threshold than the periphery to optimize dynamic refresh characteristics. Peripheral transistors are optimized at reduced threshold values for maximum high speed performance. The conventional solution, therefore, is to separately adjust the threshold of these two groups of transistors using a photomasking level (Lowrey, col. 2, ll. 4-13).

When these two teachings are read together, we generally agree with the Examiner that the skilled artisan would have readily adjusted the threshold of two different devices (i.e., access and peripheral devices) by selectively implanting a halo implant using a common mask (i.e., the polysilicon layer noted above). But we fail to see how these teachings reasonably suggest providing three or more of such devices with respective different threshold values using the claimed technique.

At best, Lowrey teaches masking n-channel areas (i.e., areas over n-wells 21) to selectively apply a halo implant to p-type material. While we can see how such a technique would achieve two different threshold voltages

resulting from the presence or absence of a halo implant, we fail to see how such a technique would result in three or more threshold voltages for three different devices. Nor has the Examiner explained on this record how this can be achieved.

In our view, using the claimed technique to conduct halo implants using a common mask to impart to at least three different devices three different threshold voltages goes well beyond mere duplication of parts. The claimed invention uses a common mask for three different devices to vary the degree of masking which dictates the resulting halo implant. In short, the type of mask dictates the type of halo implant. The particular type of halo implant that is formed, in turn, dictates the resulting threshold voltage for that particular device. That is the essence of the claimed invention.

As shown in Figure 6 of the present application, partial masking (partial exposure) for transistor 26 results in only one halo region 41. Complete masking (no exposure) for transistor 26a results in no halo region at all. But no masking (full exposure) for transistor 26b results in two halo regions 41. As a result, transistor 26b has the highest threshold voltage and transistor 26a has the lowest threshold voltage. The threshold voltage of transistor 26 is between that of the other transistors. *See* Specification 9, l. 1 - 10, l. 16.

To render the claimed invention obvious over Lowrey, the skilled artisan would have to recognize that the common mask (polysilicon 45) could somehow be altered to provide at least three different exposure levels that would result in at least three different types of halo implants for three or more discrete devices respectively. Such an alteration of the structure of Lowrey, in our view, simply strains reasonable limits and amounts to

impermissible hindsight reconstruction of the invention using Appellant's own disclosure as a blueprint.

Although the Examiner contends that DRAMs typically include hundreds of different transistors with different threshold voltages, such as read-out transistors (Answer 6), the Examiner has provided absolutely no evidence on this record to support this assertion apart from mere conclusory statements. In any event, even if we assume that DRAM devices include numerous devices distinct from the peripheral and access devices as the Examiner asserts, Lowrey still falls well short of teaching providing different threshold voltages for these other devices using the particular common mask technique recited in the claims.

In sum, Lowrey reasonably suggests adjusting the threshold voltage of two devices by selectively applying a halo implant via masking. But this teaching merely suggests that the implant is either applied or it is not -- a binary implantation that provides, at best, two different threshold voltages. Lowrey does not, however, reasonably teach or suggest varying the degree of masking to vary the degree of resulting halo implant regions (and the resulting threshold voltages) to achieve three or more threshold voltages, let alone associating each such threshold voltage with a different device respectively.

For the foregoing reasons, we will not sustain the Examiner's rejection of claims 11, 12, and 14.

DECISION

We have not sustained the Examiner's rejection with respect to all claims on appeal. Therefore, the Examiner's decision rejecting claims 11, 12, and 14 is reversed.

REVERSED

KIS

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